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Barrier Height Calculation of Ag/n-ZnO/p-Si/Al Heterojunction Diode

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ABSTRACT: The Ag/n-ZnO/p-Si(100)/Al heterojunction diodes are fabricated by pulsed laser deposition of ZnO thin films are on p-Si. High purity vacuum evaporated silver and aluminum metals were used to make contacts to the n-ZnO and p-Si, respectively. The current–voltage characteristics of Ag/n-ZnO/p-Si(100)/Al structure measured over the temperature range 80-300K have been studied on the basis of thermionic emission diffusion mechanism. The Schottky barrier height and diodes ideality factor are determined by fitting of measured current–voltage data in to thermionic diffusion equation. It is observed that the barrier height decreases and the ideality factor increases with decrease of temperature and the activation energy plot exhibit non-linear behavior. This decrease in barrier height and increase in ideality factor at low temperature are attributed to the occurrence Gaussian distribution of barrier heights. The capacitance–voltage characteristics of Ag/n-ZnO/p-Si(100)/Al heterojunction diode are also studied over the wide temperature range.

Keywords: Current-voltage and Capacitance-voltage characteristics; Ag/n-ZnO/p-Si/Al heterojunction; Barrier height and Ideality factor.

INTRODUCTION: Zinc oxide (ZnO) is a direct band semiconductor; with wide band gap (3.37eV) and large excitation binding energy (60mV) have been attracted considerable attention of the researchers due to the potential applications in optoelectronic devices, spintronics, photovoltaic and sensors [1-4]. The ZnO is popular because of its natural abundance, non-toxic nature and low cost [5]. Developing a high performance ZnO based optoelectronic devices requires forming perfect Schottky or Ohmic contacts between ZnO and metal system. ZnO thin film have been deposited using a number of different techniques such as pulsed laser deposition (PLD) [6], radio frequency (RF) magnetron sputtering [7,8], chemical vapour deposition (CVD) [9,10], spray pyrolysis [11] and sol-gel spin coating technique [12,13]. Among them, the PLD technique is very unique for the growth of oxide materials because the oxygen plasma created by the pulsed laser is very energetic and its density is easily controllable by changing the oxygen pressure. PLD enables the production of high quality ZnO films at lower temperatures than other methods due to the high energy of ablated particles in the laser produced plasma plume [14-16]. Gupta et al. [17] was deposited ZnO thin films on silicon substrates by ablating ZnO target (99.99% pure) with a KrF laser (248nm, 15 ns, 20 Hz) and studied the influence of deposition parameters on the film quality.

The best films were obtained using laser fluencies around 2.75 Jcm^{-2} and the substrate temperature T_S of 250°C. The morphology of ZnO films deposited at low oxygen pressures (10^{-3} – 10^{-2} Pa) exhibited 3D growth features evidenced by well-faceted hexagons. The use of heterostructure provides an advantage in the control of the electronic and optoelectronic properties of semiconductor devices [18] a number of significant studies, especially on photodiode properties of n-ZnO/p-Si heterojunctions, have been carried out on the fabrication of ZnO-based heterojunctions. Farag et al. [19] fabricated Al/ZnO/p-Si/Al heterojunction and determined the barrier height to be 0.56eV. Zhang et al. [20] studied the Ag/ZnO schottky barrier diodes on F-doped SnO_2 glass substrates and determined the barrier height to be 0.85eV and 1.68eV (100 KHz) by current-voltage and capacitance-voltage measurements, respectively. Keskenler et al. [13] studied the Ag/ZnO/pSi/Al Schottky diode and determined the barrier height to be 0.71eV. In this work, we have fabricated the Ag/n-ZnO/p-Si/Al Schottky diode and studied the optical properties, temperature dependent

I-V and C-V characteristics in the temperature range 80-300K.

MATERIALS AND METHOD: The ZnO/p-Si heterojunction diode was fabricated on boron doped p-type (1 Ω-cm resistivity) silicon wafer of (100) orientation. The p/p^+ silicon wafer had an 8.9μm epitaxial p layer over the heavily doped p^+ region. Prior to back ohmic contact and Schottky contact deposition, the silicon wafer was properly cleaned and etched for native oxide removal from the surface. The wafer was first cleaned with organic solvents viz., trichloroethylene, acetone and methanol in succession and then rinsed in demonized water of resistivity 18 MΩ cm and then etched in a 40% HF solution for one minute. After each cleaning step, the silicon wafer was rinsed thoroughly in demonized water of resistivity 18 MΩ for 1 minute. After cleaning and etching steps, the silicon wafer was loaded in 12" vacuum coating unit Model 12A4D. The Ohmic contact was established on the back (i.e. the p^+- side) side of the silicon wafer by depositing high purity (99.999%) aluminum at a pressure of 3×10^{-6} mbar with a thickness of ~2000A˚. Thereafter the back ohmic contact was annealed at 300˚C for 1 hour in a vacuum of 1×10^{-3} mbar.

Prior to deposition ZnO on front side i.e. on p-side, the silicon wafer with ohmic contact is cleaned and etched in a 40% HF solution for one minute for removal of native oxide layer formed on silicon. The back ohmic contact metal is protected from etching by coating a layer of picein on it. The ZnO film is deposited on the front side of p-type silicon by pulsed layer deposition technique. The Silver film (thickness ~2000A˚) was subsequently deposited by 12" vacuum coating unit Model 12A4D onto the ZnO, through holes of 1mm diameter in the metal mask in a vacuum of 3×10^{-6} mbar to form a heterojunction diode. For the electric characterization, the temperature dependent I-V measurements are performed by a programmable Keithley 2400 source meter in the temperature range of 80-300K using a Lakeshore 331 temperature controller and close cycle helium refrigerator system. The whole I-V measurements were performed using a data acquisition program on a personal computer through an IEEE-488 interface card. The C-V measurements were performed on a precision impedance analyzer (Wayne Kerr 6520A).

RESULTS AND DISCUSSION: The ln(*I*)-*V* characteristics of Ag/ZnO/p-Si/Al heterojunction diodes in the temperature range 80-300K are shown in Fig. 1. These ln(*I*)-*V* plots show that the Ag/ZnO/p-Si/Al heterojunction diodes exhibits good rectification behavior over wide temperature range. Near room temperatures, the linear portion is observable only over low bias range. It is probably due to low barrier height of the heterojunction. At low temperature these plots clearly exhibits linearity over several order of current. Further, they progressively become straight over a wide bias range with decrease in temperature. The increase of the straight-line portion of the ln(*I*)-*V* curve and their gradual shift towards higher bias side with decrease in temperature are in agreement with thermionic emission diffusion Eq. (1).

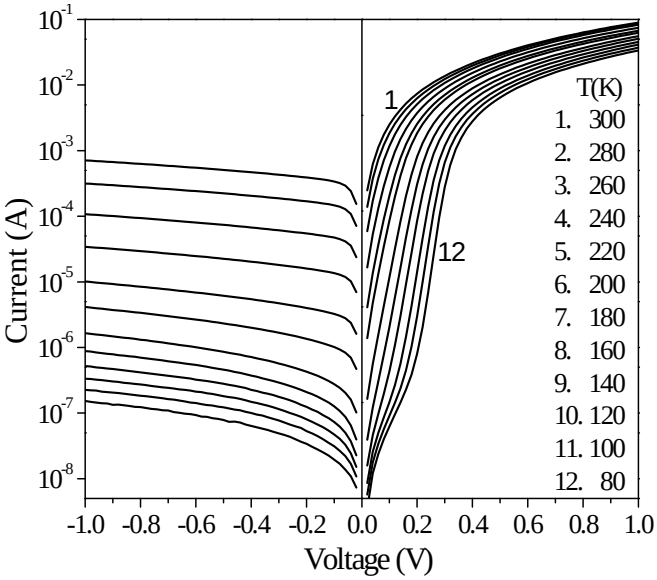

Figure 1: Current-voltage characteristics of Ag/n-ZnO/p-Si/Al heterojunction diodes at various temperatures.

$$I = I_S \exp\left(\frac{q(V - IR_S)}{\eta kT}\right)\left[1 - \exp\left(\frac{-q(V - IR_S)}{kT}\right)\right], \qquad (1)$$

with

$$I_S = A_d A^{**} T^2 \exp\left(\frac{-q\phi_{b0}}{kT}\right), \qquad (2)$$

Where; $I_s$is saturation current at zero bias, A_d is the diode area, *A*** is the effective Richardson constant, T is the temperature in Kelvin, *k* is the Boltzmann constant, *q* is the electronic charge, ϕ_{b0} is the zero-bias barrier height, η is the ideality factor and R_s the diode series resistance.

It is customary to extract from the straight-line portion of the ln(I)-V plots the saturation current (I_s) by extrapolation to zero-bias and the ideality factor from the slope itself. Also, R_s data are found from the best fit of experimental *I-V* data in Eq. (1) by least square fitting method. Alternatively, a computer program is utilized to fit the experimental *I-V* data in the thermionic Eq. (1) by iteration, takingI_s , η and R_s as adjustable parameters. Once I_s is known, the barrier height ϕ_{b0} can easily be determined from Eq. (2) at any temperature for a given diode area A_d and

Richardson constant *A**** ($3.2\times10^5 Am^{-2} K^{-2}$ for *n- ZnO* and *p-Si)* [13, 20].

The zero bias barrier height obtained by fitting of experimental I-V data in to Eq. (1) are shown in Fig. 2. The zero-bias barrier height ϕ_{b0} decreases from 0.468V at 300K to 0.249sV at 80K. The zero-bias barrier height show decreases rapidly at low temperature.

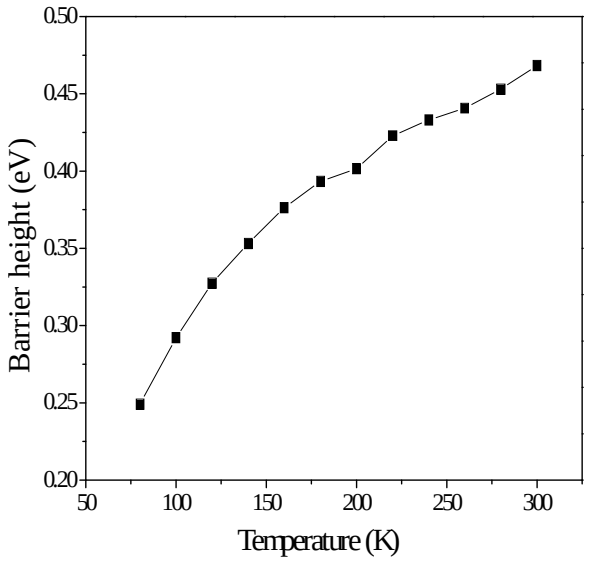

Figure 2: Barrier height as a function of temperature for Ag/n-ZnO/p-Si/Al heterojunction diode.

The variation of ideality factor with temperature is shown in Fig. 3. The extracted ideality factor is relatively higher near room temperature because the ln(I)-V plots have much less linear region. However at lower temperature below 260K the linear portion increases and the derived ideality factor is also low.

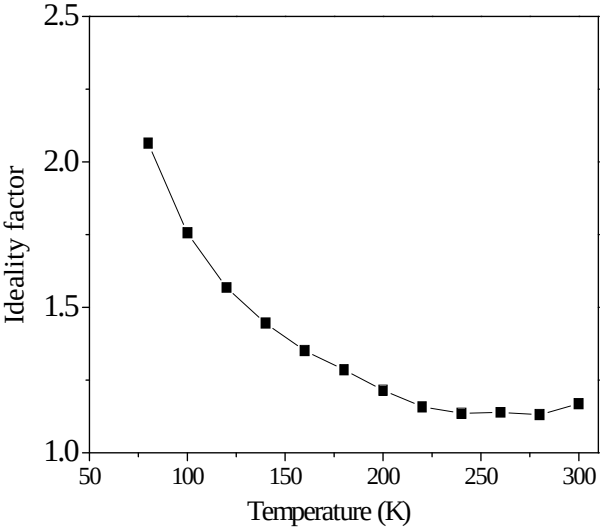

Figure 3: Ideality factor as a function of temperature for Ag/n-ZnO/p-Si/Al based Schottky contacts.

$$\ln\left(\frac{I_S}{T^2}\right) = \ln\left(A_d A^{**}\right) - \frac{q\phi_{b0}}{k}\frac{1}{T} \qquad (3)$$

Below this temperature the ideality factor initially increases marginally with decrease in temperature and significantly below 140 K acquiring a value of 2.06 at 80K. The barrier height can also be determined in yet another way from the activation energy plot. For this Eq. (2) can be expressed as

Therefore, the $\ln(I_s/T^2)$ versus 1/T plot should, yield a straight line, the slope of which determines the zero bias barrier height ϕ_{b0} and the intercept at the ordinate giving the Richardson constant for known diode area A_d. This method gives a single value of barrier height from the entire I-V data over the entire temperature range. Fig. 4 shows the plot of $\ln(I_s/T^2)$ versus 1000/T obtained from the experimental I-V data at various temperatures. The plot shown in Fig. 4 is not a linear, however, it can be fitted in a straight line at higher temperature region and at low temperature the plot deviates from linearity. The activation energy obtained from the linear portion at higher temperature is 0.27eV, and the Richardson's constant A** obtained from the intercept of the straight portion at the ordinate is equal to 1.74×10^2 $Am^{-2}K^{-2}$, which is much lower than the known value of 3.2×10^5 $Am^{-2}K^{-2}$. The decrease in barrier height, increase in ideality factor with decrease in temperature and nonlinear behavior of activation at low temperatures are at first sight indicative of deviation from the pure thermionic emission-diffusion mechanism and needs further investigation.

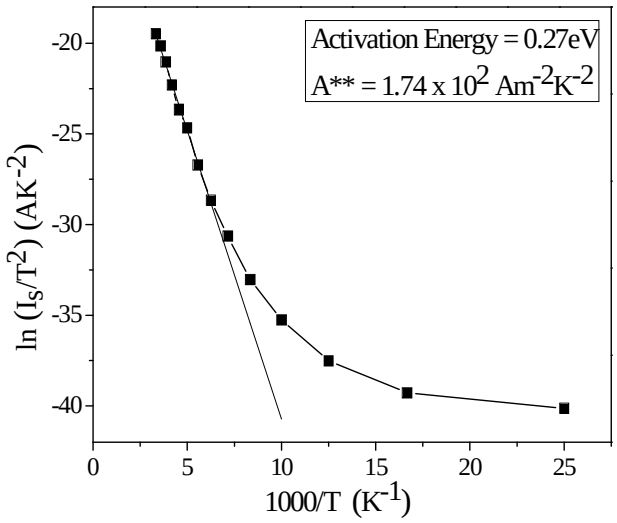

Figure 4: Conventional activation energy ($\ln(I_s/T^2)$ vs. 1000/T) plot of Ag/n-ZnO/p-Si/Al heterojunction.

The significant decrease of zero-bias barrier height and increase of ideality factor especially at low

temperatures are possibly caused by barrier heights (BH) in homogeneities resulting due to variation in thickness and composition of ZnO film. Describing the BH in homogeneities with a Gaussian distribution function, Eqs (1) and (2) get modified in such a way that ϕ_{ap} appear in place of ϕ_{b0} [33-34]. The ϕ_{ap} is termed as apparent zero-bias barrier height and is given by

$$\phi_{ap} = \bar{\phi}_{b0} - \frac{q\sigma^2}{2kT} \quad (4)$$

Where; $\bar{\phi}_{b0}$ stands for mean zero bias barrier height and σ is the standard deviation of Gaussian distribution of barrier heights. In order to see the occurrence of Gaussian distribution of barrier heights in Ag/n-ZnO/p-Si/Al zero bias barrier height is plotted as function of 1/T and is shown in Fig. 5. Clearly data fit well in form of a straight line which indicates the occurrence of Gaussian distribution of barrier height. The slope of this may be used to derive mean of the distribution σ and the intercept on ordinate yields the value of the zero bias mean barrier height $\bar{\phi}_{b0}$.

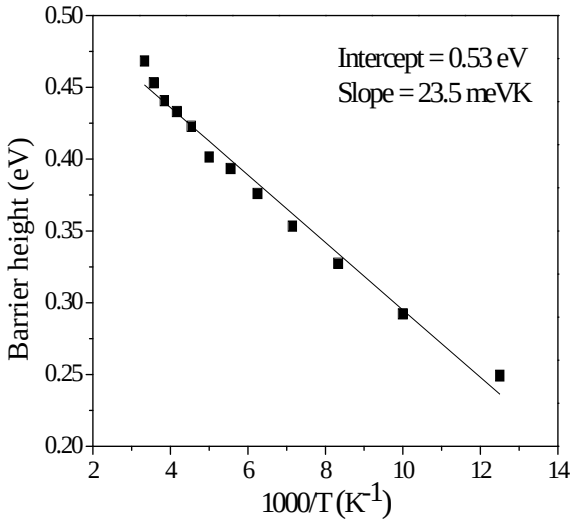

Figure 5: The barrier height ϕ_{ap} obtained from I-V measurements as a function of inverse temperature.

The intercept of the best fit yields mean barrier height which is found to be 0.53eV. From the slope of the best fit straight line the value of standard deviation of the distribution is evaluated to be 0.064V. Thus, it is obvious that the decrease of zero-bias BH is caused, by the existence of the Gaussian distribution of barrier heights. Substituting the value of ϕ_{ap} in Eq. (3), the modified activation plot

$$\ln\left(\frac{I_S}{T^2}\right) - \frac{q^2\sigma^2}{2K^2T^2} = \ln\left(A_d A^{**}\right) - \frac{q\phi_{b0}}{kT} \quad (5)$$

The Fig. 6 shows the modified activation energy plot along with the original activation energy plot. Clearly the modified activation energy plot exhibits a straight line over entire temperature range of measurement from 300 K down up to 80 K. The Richardson's plot obtained from the modified activation energy plots is found to be 5.29×10^5 $Am^{-2}K^{-2}$, in close agreement with the known value of 3.2×10^5 Am^{-2} K^{-2}, and the barrier height obtained is 0.54eV.

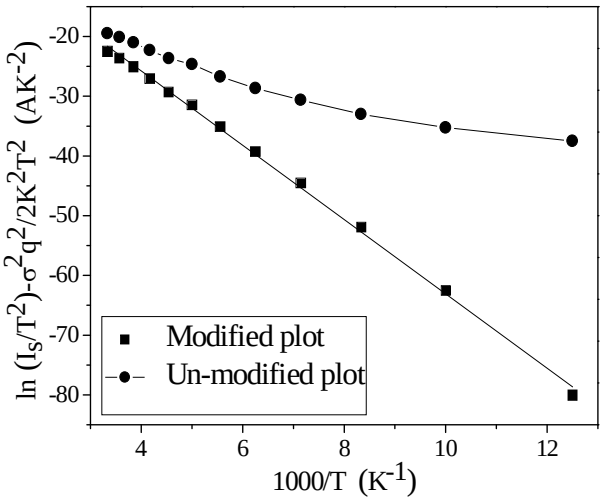

Figure 6: Modified activation energy plots corresponding to the standard deviation σ equal to 0.064 V is shown in figure.

The capacitance of Ag/n-ZnO/p-Si/Al heterojunction diode was measured as function of reverse bias at various temperatures. The C-V characteristics have been analyzed using the Schottky-Mott equation [21, 22]

$$\frac{1}{C^{-2}} = \frac{2}{A^2}\left(\frac{V_{bi}+V}{q\varepsilon_S N_{eff}}\right) \quad (6)$$

Where; A is the diode area, q is electronic charge, ε_s is the dielectric constant of semiconductor, $\varepsilon_0$is the dielectric constant of free space, V_{bi} is the built-in voltage of the diode and V is the applied voltage and N_{eff} is the effective doping density, given as:

$$\frac{1}{N_{\text{eff}}} = \frac{1}{N_D} + \frac{1}{N_A} \quad (7)$$

Where; N_D is the donor impurity concentration in ZnO and N_A is the acceptor concentration in p-type silicon. Fig. 7 shows the C^{-2} versus V plots of the Ag/n-ZnO/p-Si/Al heterojunction diode at various temperatures at frequency 1MHz. The built-in voltage can be determined as the intercept of this plot on the C^{-2} axis. The value of N_{eff} is estimated to be 7.12×10^{15}/cc. As the p-type silicon on which the ZnO is deposited is having resistivity 1Ω-cm which

corresponds to the acceptor density equal to 1.3×10^{16}/cc. From these values of N_{eff} and N_A the donor concentration in n-ZnO is estimated to be ~1.57×10^{16}/cc.

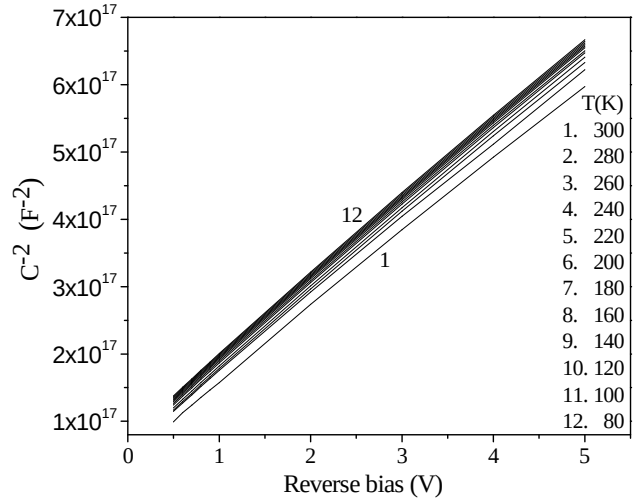

Figure 7: The $\frac{1}{C^2}$ *vs* V characteristics of the Ag/n-ZnO/p-Si/Al heterojunction diode at a frequency of 1MHz at various temperatures.

The equivalent Schottky barrier height is derived from the built-in barrier as [43]

$$\phi_b = V_{bi} + \frac{kT}{q} + \frac{kT}{q}\ln\left(\frac{N_V}{N_A}\right) \qquad (8)$$

Where; *k* is the Boltzmann constant, *T* is temperature, N_V is the effective density of states in the valance band, and is given by [22, 23]

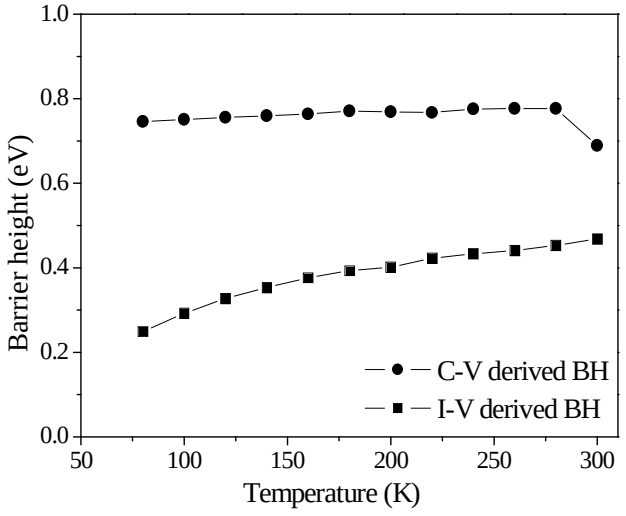

Figure 8: Barrier height derived from the C-V and I-V measurements of the heterojunction diode at 1 MHz frequency.

$$N_V = 2\left(\frac{2\pi\, m_h^* kT}{h^2}\right)^{\frac{3}{2}} \qquad (9)$$

Here, m_n^* is the effective mass of an electron and 'h'is Plank's constant. The barrier height is estimated from built-in barrier using Eq.(9).

The barrier heights derived from the capacitance-voltage data of the Ag/n-ZnO/p-Si/Al heterojunction are shown in Fig. 8 along with the barrier height derived from the I-V data. Clearly the barrier height derived from the C-V data is larger than the barrier height derived from the I-V data.

As expected, the barrier height values derived from the C-V measurement are higher than those obtained from the I-V measurements. This discrepancy can be explained by the different nature of the C-V and I-V measurement techniques. The barrier heights deduced from two techniques are not always the same. If the barriers are uniform and ideal, the two measurement yields the same value; otherwise, they will yield different values. The different behavior of Schottky barrier height obtained from the two techniques can be explained by a distribution of Schottky barrier height due to the inhomogeneities that occur at metal-semiconductor interface [23, 24]. In addition, the C-V technique averages over the whole area and measure the barrier height of Schottky diode. On the other hand, the barrier height from the I-V method includes any barrier lowering effect due to the interfacial insulator layer or the interface states and an effective barrier height is measured. Other than this, the determination of Schottky barrier height from I-V characteristics is only reliable if one can be confident that the current is determined by TE theory. For this to be so, forward portion of the characteristics must be a good straight line with low value of ideality factor [25, 26].

CONCLUSION: The Ag/n-ZnO/p-Si/Al heterojunction diodes are fabricated by pulsed laser deposition technique. Forward *I-V* characteristics of the Ag/n-ZnO/p-Si/Al heterojunction are interpreted in terms of thermionic emission-diffusion mechanism to find the equivalent barrier height. While the zero-bias barrier height ϕ_{b0} decreases the ideality factor increase with decrease in temperature, the changes being quite significant at very low temperatures. The zero-bias barrier height of Ag/n-ZnO/p-Si/Al heterojunction diodes from the activation energy fit at higher temperature is found to be ~0.27 eV and the$\ln(I_s/T^2)$ vs 1000/T plot shows deviation from linearity at low temperatures. Barrier height inhomogeneities concept is used it explain the decrease of barrier height and increase of ideality factor at low temperatures. The inhomogeneities can be described by the Gaussian distribution of barrier

heights with mean barrier height of 0.53eV and standard deviation 0.064 V**.**

The capacitance-voltage characteristics of the Ag/n-ZnO/p-Si/Al heterojunction diode at 1 MHz frequency were measured in the temperature range 80-300K. The built-in barrier and the barrier height of Ag/n-ZnO/p-Si/Al heterojunction diode were also obtained from C-V measurements. The impurity concentration in n-ZnO was estimated to be 1.57×10^{16} per cc.

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